Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VCC**
2. **G-N.A**
3. **A**
4. **H-N.B**
5. **B**
6. **I-N.C**
7. **C**
8. **VSS**
9. **D**
10. **J-N.D**
11. **E**
12. **K-N.E**
13. **NC**
14. **F**
15. **L-N.F**

**.057”**

**12**

**11**

**4**

**5**

**3 2 1 15 14**

**6 7 8 9 10**

**MASK**

**REF**

**CD E**

**.058”**

**NOTE: BOND FIRST WIRE TO VSS – BOND PAD #8**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC**

**Mask Ref: E**

**APPROVED BY: DK DIE SIZE .057” X .057” DATE: 8/25/21**

**MFG: FAIRCHILD THICKNESS .014” P/N: CD4049UB**

**DG 10.1.2**

#### Rev B, 7/1